ABSTRACT OF THE DISCLOSURE

A semiconductor device evaluation method and apparatus are provided which do not require a measurer to expend a great deal of time and effort even when measuring a large number of points, can prevent the occurrence of variations in measured values from measurer to measurer, and allow the measurement of the finished gate length even if gate pattern does not appear on the semiconductor device surface. There is also provided a semiconductor device manufacturing control method which applies such an evaluation method and apparatus to the control of semiconductor device manufacturing. For a plurality of insulated gate transistors with different channel lengths, an effective channel length (Leff), a gate capacitance (Cg), and a fringing capacitance (Cf) are determined by electrical measurement and/or calculation. The gate capacitance (Cg) and the effective channel length (Leff) are extended on a graph by extrapolation to determine gate-capacitance-vs.-effective-channel-length characteristics. Then, a gradient (A) of the characteristics is calculated to determine the finished gate length (Lg) for each of the plurality of insulated gate transistors from the equation, $Lg = (Cg - Cf)/A$.